

## BRIEF DESCRIPTION OF THE DRAWING

Page 4, lines 18 to 19, please make the following changes:

~~An exemplary embodiment of the present invention is shown in Figure 1 and will be described in greater detail below[.].~~

The objects, features and advantages of the invention will now be illustrated in more detail with the aid of the following description of the preferred embodiments, with reference to the accompanying figures in which:

Figure 1 is a schematic circuit diagram of an intermediate-circuit bus of a frequency converter with a monitoring circuit according to the invention for detecting short circuits in capacitor units; and

Figure 2 is a schematic circuit diagram of an intermediate-circuit bus with a plurality of monitoring circuits for detecting short circuits in a plurality of capacitor units.

Page 4, line 20, please insert the following heading:

## DETAILED DESCRIPTION OF THE INVENTION

Page 5, lines 4 to 15, please make the following changes:

The monitoring circuit (16) is preferably composed of two series-connected resistors (3,4), four diodes (5), (6), (7), (8), a zener diode (15), and an electrically isolated ~~a galvanically insulated~~ output (12). In this case, the ~~galvanic insulation~~ (9) electrical isolation (9) is realized by a combination of a light-emitting diode (17) and a light-sensitive transistor (18), the transistor including an open collector

output (12). Diodes (5) and (6), and (7) and (8) are connected in series, whereby the cathode of diodes (5) and (8) is connected to the anode of diodes (6) and (7). The two diode pairs are then connected in parallel, so that the cathodes of the diodes (6) and (7) ~~6 and 7~~ are connected with each other, and the anodes of diodes (5) and (8) are connected with each other. The connection between diodes (5) and (6) is connected to the capacitor voltage to be measured. The connection point between diodes (7) and (8) is connected to the reference voltage.

Page 6, lines 1 to 7, please make the following changes:

When a capacitor (2,1) short circuits, a voltage difference ~~differential voltage~~ forms between junctions (13) and (14). When this voltage difference ~~differential voltage~~ exceeds a predefined threshold that corresponds to the sum of two diode voltages (7,5) or (6,8) plus the zener diode (15) breakthrough voltage, current flows. The circuit is designed so that current always flows through the zener diode (15) in the same direction, independently of whether the voltage at junction (13) ~~13~~ is greater than or less than the voltage at junction (14) ~~14~~.

Page 6, lines 9 to 24, please make the following changes:

The current resulting from the voltage asymmetry activates the light-emitting diode (17), which switches the transistor (18) ~~(9)~~ on, thereby activating the error signal (12). The strength of the current is limited by the size of the resistor (3) and/or (4). Since the properties of zener diodes and light-emitting diodes are

dependent on the current intensity, the components must be designed such that a rapid activation of the error signal (12) is ensured. When a plurality of capacitors (1,2) is connected in series, then, to ensure that the individual capacitors (1,2) are monitored, the monitoring circuit must be present in plurality, i.e., an additional monitoring circuit must be installed for each additional series-connected capacitor. This is shown in Figure 2, whereby the four 4-capacitors (1) are monitored by three 3-monitoring units (19). One error signal output (12), one reference voltage input (14) and an associated capacitor voltage input (13) are provided for each unit. Activation of an error signal (12) is still caused by a capacitor short circuit (1), whereby the short-circuiting of a capacitor (1) can trigger one or more error signals (12). All error signals (12) should be monitored so that, if a short circuit occurs, it is possible to determine exactly which capacitor (1) has failed.

Page 7, please delete this page, i.e. the parts list in its entirety.

## **REMARKS**

### **I. Objection to the Specification**

The disclosure was objected to because there were no headings provided in the specification and because the term "claim" was used in the specification on page 1, line 5, page 2, lines 1 and 14.

References to the claims by number are not permitted according to the rules. Thus the reference to the claims has been deleted from the specification.

Standard section headings were added in accordance with the U.S. Patent Office Rules.

The specification was object to for failing to provide proper antecedent basis for claims 12 and 13. It is respectfully submitted that this objection was incorrect. Individual capacitors are referred to on pages 4 and 6 of the specification. The same is true of the resistors. Also claims 12 and 13 have been canceled, obviating any rejection based on their specification wording. New wording has been used in the new claims.

Also a "Brief Description of the Drawing" section has been added to the specification, in accordance with the rules.

For consistency all the drawing reference numbers have been provided with parentheses in the detailed description.

Some minor translation and other wording errors were corrected.

For the foregoing reasons and because of the changes in the specification and claims withdrawal of the objection to the disclosure is respectfully requested.

## **II. Drawing Figures**

Figures 1 and 2 were objected to for not including legends.

Replacement sheets including figures 1 and 2 were provided with the required legends corrected under 37 C.F.R. 1.121 (d).

Because of the corrections in figures 1 and 2, withdrawal of the objection to the figures is respectfully requested.

## **III. Claim Objections**

Claims 14 to 25 have been added and the original claims 1 to 13 were canceled.

The original claims were English translations of claims of a foreign patent. The new claims have been drafted in accordance with the suggestion in paragraph 6 on page 5 of the Office Action. The new claims 14 to 25 have been drafted in accordance with US Patent Office Rules.

Also these claims have been checked for compliance with 35 U.S.C. 112, second paragraph.

#### IV. Anticipation Rejection

Claims 1 to 3, 5 and 7 to 9 were rejected as anticipated under 35 U.S.C. 102 (b) by Kataoka, et al.

Kataoka, et al, does disclose a monitoring circuit for detecting faults, such as short circuits, in a DC capacitor circuit. However this monitoring circuit differs in significant structural ways from the applicants' monitoring circuit claimed in the new claim 14.

The original claims were English translations of claims of a foreign patent. The new claims 14 to 25 have been drafted in accordance with the suggestion in paragraph 6 on page 5 of the Office Action and in accordance with US Patent Office Rules.

New claim 14 claims a monitoring circuit as a collection of cooperating means for performing certain functions, which were included in the canceled claim 1. The monitoring circuit of new claim 14 comprises

means for deriving a reference voltage (14) from an intermediate-circuit voltage (L(+), L(-)) applied across said at least two series-connected capacitor units (1, 2);

means for generating a control signal consisting of a voltage difference between said reference voltage (14) and a junction voltage at a junction (13) between two of said capacitor units (1, 2); and

means for generating an error signal when said voltage difference falls

*below or exceeds an activation threshold voltage thus indicating that said one of said capacitor units (1,2) has been short-circuited.*

The italicized functions are recited in the canceled claim 1, except that the term "shunting" is used, instead of "deriving" with regard to the manner in which the reference voltage is produced.

The "means for" wording was necessary to convert a recitation of the steps of the method of operation of the monitoring circuit into device components. The structure of these device components is described in applicant's specification, especially detailed description in reference to the figure 1 and in dependent claims. This description full supports the new claim 14.

Kataoka, et al, do not disclose the feature that *"a control signal is produced consisting of a voltage difference between said reference voltage (14) and a junction voltage at a junction (13) between two of said capacitor units (1, 2)"* Instead Kataoka, et al, generate a control signal consisting of a voltage difference between a junction between DC capacitors 11a and 12a and a junction between DC capacitors 11b and 12b. See column 2, lines 40 to 45. However the figure of Kataoka, et al, do show a reference voltage  $V_{ref}$ , although the manner in which it is produced is not described.

Also Kataoka, et al, do not derive *a reference voltage (14) from the voltage  $V_E$  applied across the capacitor units (1, 2)* shown in fig. 2 of Kataoka, et al. The manner of producing the reference voltage,  $V_{REF}$ , is not described in Kataoka, et al. A reference voltage by its nature differs from the voltage at the junctions described in Kataoka, et al, because the voltage at the junctions can

vary with the operating conditions.

It is well established that each and every limitation of a claimed invention must be disclosed in a single prior art reference in order to be able to reject the claimed invention under 35 U.S.C. 102 (b) based on the disclosures in the single prior art reference. See M.P.E.P. 2131 and also the opinion in *In re Bond*, 15 U.S.P.Q. 2nd 1566 (Fed. Cir. 1990).

First, Kataoka, et al, do not disclose means or structure that perform the functions of the three components included in new claim 14.

In addition, the "means for" components of claim 14 must be interpreted according to the 6<sup>th</sup> paragraph of 35 U.S.C. 112 as being limited to the specific embodiments recited in the applicants' specification *or equivalents thereof*.

Even if the wording of the new claim 14 is interpreted overly broadly so that the three functions performed by the "means for" components recited in new claim 14 are identified with functions performed by various parts of the Kataoka, et al, monitoring device, claim 14 is still not anticipated by Kataoka, et al.

The applicants' means for components are structured differently and operate in different ways from the components of Kataoka, et al. For example, the "means for" generating the error signal includes the light-emitting diode/light-sensitive transistor pair, which is not disclosed or suggested in Kataoka, et al. Also the "means for" generating the control signal is simpler and more rapidly activated than the corresponding elements of the circuit of Kataoka, et al, because it does not involve the comparator circuits shown in the circuit diagram of Kataoka, et al. Instead it includes a set of diodes and a zener diode.



In order for the "means for" components of a claimed invention to be equivalent to corresponding prior art "means for" components they must perform their functions in the same manner as the prior art components or have insubstantial differences between them. That is not the situation here as noted above. See M.P.E.P. 2184. II "Factors to be considered in Deciding Equivalence".

It is respectfully submitted that the structure of the monitoring circuit 16 of the applicants with the Zener diodes and the light-emitting diode and light-responsive transistor shown in applicants' figure 1 is not equivalent to that of the corresponding monitoring circuit means of Kataoka including the comparator circuit 15 and window comparator 19, which receives the VREF.

For the foregoing reasons and because of the new wording in the new claims it is respectfully submitted that new claims 14 to 25 should not be rejected under 35 U.S.C. 102 (b) as anticipated by Kataoka, et al.

#### **V. Obviousness Rejections**

Claims 4 and 6 were rejected under 35 U.S.C. 103 (a) as obvious over Kataoka, et al, in view of Lumbroso.

Dependent claim 16 contains the features of canceled claim 4.

Kataoka, et al, do describe a monitoring circuit for reporting faults that occur in a DC monitoring circuit, more specifically for reporting faults in the capacitors, such as short circuits. The faults or short circuits are signaled or

reported as quickly as possible without a time delay on the basis of a detected voltage difference between parts of the circuit, in fact respective junction points between series connected capacitors.

Lumbroso discloses a monitoring circuit for monitoring a fuel level measuring device for a fuel tank of a motor vehicle. When the fuel level reaches 0, the monitoring device will light an emergency light indicating that there is no more fuel. However it is not desirable to have the monitoring circuit light the emergency light at the instant the input current or voltage level signals that the no-fuel condition is reached. The reason is that that condition can be the result of a false indication due to a tilted or tipped condition of the vehicle that occurs when the vehicle passes around a curve at high speed. During this latter transient condition the monitoring circuit would incorrectly indicate a zero fuel level when the vehicle passed around the curve at high speed. Hence it was necessary to build a time delay means into the monitoring circuit which signals a zero fuel level in the tank in order to avoid a transitory false or flickering indication of a no fuel condition.

Lumbroso builds a time delay device into their monitoring circuit in order to provide the required time delay between onset of the no-fuel input signal and the warning signal comprising illumination of the warning light. The time delay device is described on page 2, left hand column, lines 8 to 45. The time delay device comprises a capacitor C connected in series with resistor R, a thyristor TH connected in parallel with the series connected resistor R1 and capacitor C and a zener diode connected between the gate of the thyristor and the junction point

between the capacitor C and the resistor R1.

The zener diode controls the time point at which the warning light goes on, because, as explained between lines 35 to 41 of the left hand column of page 2 of the GB reference, the nominal or breakdown voltage of the zener diode controls the time at which the thyristor becomes conducting and thus the warning light lights.

For the foregoing reasons it should be absolutely clear that one skilled in the art would have no motivation to include either the time delay circuit device of Lumbroso or the zener diode of Lumbroso in the monitoring circuit of Kataoka, et al. The monitoring circuit of Kataoka, et al, requires no time delay device because the faults or short circuits should be reported at the instant they happen. On the other hand, the time delay device with the zener diode has a useful purpose in the monitoring device of Lumbroso for indication the fuel level in a motor vehicle fuel tank.

Thus the suggestion in the prior art to combine these two references under 35 U.S.C. 103 (a) in the suggested manner is lacking. There is no reason that one skilled in the art would include the zener diode of Lumbroso in the circuit of Kataoka, et al, at least without the applicants' disclosure as a guide which is not permitted under 35 U.S.C. 103 (a). For example, the Federal Circuit Court of Appeals has said:

"The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification...It is impermissible to use the claimed invention as an instruction manual or "template" to piece

together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that "one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fritch*, 23 U.S.P.Q. 2nd 1780, 1783-84 (Fed. Cir. 1992).

The monitoring circuit of Kataoka, et al, is complete without the zener diode and performs its intended function of monitoring a DC capacitor circuit for faults in an instantaneous manner. A time delay device or zener diode is not necessary. There is no motivation in the references to modify the monitoring circuit of Kataoka, et al, by including the zener diode.

Furthermore if a time delay device were to be included in the monitoring circuit of Kataoka, et al, it would not be able to perform its intended function. A proposed modification under 35 U.S.C. 103 (a) cannot render the art unsatisfactory for its intended purpose. See M.P.E.P.2143.01.

Considering the matter from another standpoint, the monitoring circuit of the primary reference is based on detection of a potential difference between two junction points: if a difference is detected, one of the capacitors is faulty (column 3, lines 57 to 62. It may be conceded that a zener diode might be part of a circuit that monitors the difference in potential, but there are a great variety of such circuits known in the art with a great variety of such components. There does not seem to be any particular reason that a zener diode should included and the comparators of Kataoka, et al, do not appear to include a zener diode.

Furthermore Lumbroso does not suggest the differences mentioned above in section IV between the subject matter of the new main claim 14 and the

disclosures of Kataoka, et al. For that reason new main claim 14 should be rejected under 35 U.S.C. 103 (a) over Kataoka, et al, in view of Lumbroso.

For the foregoing reasons it is respectfully submitted that new claims 14 to 25 should not be rejected under 35 U.S.C. 103 (a) over Kataoka, et al, in view of Lumbroso.

Claim 10 was rejected under 35 U.S.C. 103 (a) over Kataoka, et al, in view of Baker.

New claim 18 contains the features that were previously in claim 10.

The electrical isolation provided by the light-emitting diode/light-sensitive transistor pair is particular desirable in the preferred application of intermediate circuit bus monitored by applicants' monitoring circuit. The preferred application described in the background section of the specification involves voltages as high as 750 v. It is desirable to keep the circuit that includes such high voltages electrically isolated from the circuit that reports the faults, which is the purpose of the features of claim 18. However Baker does described a circuit including these features for monitoring a power supply.

The features of claim 18 are features of a preferred embodiment of applicants' invention, but are not currently relied on to establish patentability of applicants' claimed invention.

Furthermore Baker does not suggest the differences mentioned above in

section IV between the subject matter of the new main claim 14 and the disclosures of Kataoka, et al. For that reason new main claim 14 should be rejected under 35 U.S.C. 103 (a) over Kataoka, et al, in view of Baker.

For the foregoing reasons it is respectfully submitted that new claims 14 to 25 should not be rejected under 35 U.S.C. 103 (a) over Kataoka, et al, in view of Baker.

Claims 11 to 13 were rejected as obvious under 35 U.S.C. 103 (a) over Kataoka, et al, in view of Smith.

The features of claims 11 to 13 are features of preferred embodiments of applicants' invention, but are not currently relied on to establish patentability of applicants' claimed invention.

Furthermore Smith does not suggest the differences mentioned above in section IV between the subject matter of the new main claim 14 and the disclosures of Kataoka, et al. For that reason new main claim 14 should be rejected under 35 U.S.C. 103 (a) over Kataoka, et al, in view of Smith.


For the foregoing reasons it is respectfully submitted that new claims 14 to 25 should not be rejected under 35 U.S.C. 103 (a) over Kataoka, et al, in view of Smith.

Should the Examiner require or consider it advisable that the specification, claims and/or drawing be further amended or corrected in formal respects to put this case in condition for final allowance, then it is requested that such

amendments or corrections be carried out by Examiner's Amendment and the case passed to issue. Alternatively, should the Examiner feel that a personal discussion might be helpful in advancing the case to allowance, he or she is invited to telephone the undersigned at 1-631-549 4700.

In view of the foregoing, favorable allowance is respectfully solicited.

Respectfully submitted,



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